ABSTRACT OF THE DISCLOSURE

A phase of a sampling clock provided from clock generating circuit 107 is switched periodically and alternately with a phase difference of 180 degrees, and during a period of each phase, timing estimating circuit 105 estimates a symbol timing. High-accuracy timing estimating circuit 109 selects an estimated result with higher reliability among symbol timing estimated results obtained in respective periods, thereby enabling estimation of the symbol timing with time resolution twice a sampling period. It is possible to decrease an operation frequency in an A/D conversion circuit even in a system requiring timing synchronization accuracy with high accuracy.